IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Jens Braun

Serial No.: 10/822,529

Filed: April 12, 2004

For: METHOD AND APPARATUS FOR TESTING DRAM MEMORY CHIPS IN MULTICHIP MEMORY MODULES

§ Confirmation No.: 3329
§
§ Group Art Unit: 2138
§
§ Examiner: Saqib J. Siddiqui
§
§
§
§
§

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office to fax number 571-273-8300 to the attention of Examiner Saqib J. Siddiqui, or electronically transmitted via EFS-Web, on the date shown below:

July 11, 2007 /Randol W. Read, Reg. No. 43,876/
Date Randol W. Read

Dear Sir:

APPEAL BRIEF

Applicants submit this Appeal Brief to the Board of Patent Appeals and Interferences on appeal from the decision of the Examiner of Group Art Unit 2138 dated November 13, 2006, finally rejecting claims 1-4, 6-15 and 17-18. The final rejection of claims 1-4, 6-15 and 17-18 is appealed. This Appeal Brief is believed to be timely since it is electronically transmitted by the extended due date of July 12, 2007, as set by the filing of a Notice of Appeal on April 12, 2007. Please charge the fee of $500.00 for filing this brief to Deposit Account No. 20-0782/1525.014254 (INF/WB0077)/RWR.

TABLE OF CONTENTS

Real Party in Interest

The present application has been assigned to Infineon Technologies AG, Munich, Fed Rep Germany.

Related Appeals and Interferences

Applicant asserts that no other appeals or interferences are known to the Applicant, the Applicant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 1-4, 6-15 and 17-18 are pending in the application. Claims 1-21 were originally presented in the application. Claims 22-24 have been added during prosecution, but have not been entered for purposes of appeal. Claims 5, 16 and 19-21 have been canceled without prejudice. Claims 1-4, 6-15 and 17-18 stand finally rejected as discussed below. The final rejections of claims 1-4, 6-15 and 17-18 are appealed. The pending claims are shown in the attached Claims Appendix.

Status of Amendments

All claim amendments prior to the Final office Action have been entered by the Examiner. Proposed amendments to the claims after the final rejection were not entered.

Summary of Claimed Subject Matter

A. CLAIM 1 - INDEPENDENT

One embodiment of the invention (see, e.g., Claim 1) provides a method for testing memory cells of a DRAM memory chip arranged together with a non-volatile memory chip in a multichip memory module incorporated in an application apparatus. *See, e.g.*, Page 5, Paragraph 0017; Figure 1, Items 2, 5. The method includes conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus and providing signals, utilizing a self-test control device located within the DRAM memory chip, to a control input of the DRAM memory chip and a control input at the nonvolatile memory chip. *See, e.g.*, Page 3, Paragraph 0008; Page 5, Paragraph 0017; Figure 1, Items 2, 5. The method also includes disconnecting control input signals from outside the multichip memory module using the self-test control device. *See, e.g.*, Page 7, Paragraph 0022; Figure 1, Items 2, 5.

B. CLAIM 12 - INDEPENDENT

One embodiment of the invention (see, e.g., Claim 12) provides an apparatus for testing memory cells of a DRAM memory chip disposed with a nonvolatile memory chip in a multichip memory module incorporated in an application apparatus. *See, e.g.*, Page 5, Paragraph 0017; Figure 1, Items 1, 2, 3, 5. The apparatus includes a self-test control device, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus. *See, e.g.*, Page 3, Paragraph 0008; Page 5, Paragraph 0017; Figure 1, Items 1, 2, 3, 5. The apparatus also includes a second switching device for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module. *See, e.g.*, Figure 1, Items 1, 2, 3, 5. The self-test control device provides signals to control inputs

of the DRAM memory chip and control inputs of the nonvolatile memory chip. *See, e.g.*, Page 7, Paragraph 0022; Figure 1, Items 1, 2, 3, 5.

D. Claim 18 - INDEPENDENT

One embodiment of the invention (see, e.g., Claim 18) provides an apparatus for testing memory cells of a DRAM memory chip disposed with a nonvolatile memory chip in a multichip memory module incorporated in an application apparatus. *See, e.g.*, Page 5, Paragraph 0017; Figure 1, Items 1, 2, 3, 5. The apparatus includes a self-test control means, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus. *See, e.g.*, Page 3, Paragraph 0008; Page 5, Paragraph 0017; Figure 1, Items 1, 2, 3, 5. Figure 1, Items 1, 2, 3, 5. The apparatus also includes a central processing means, disposed outside the multichip memory module and connected to the self-test control device, for initiating the self-test and providing control commands to the DRAM memory chip. *See, e.g.*, Page 6, Paragraph 0018; Figure 1, Items 1, 2, 3, 5. The apparatus includes a switching means for deactivating a common data bus of the DRAM memory chip and of the nonvolatile memory chip outside the multichip memory module. *See, e.g.*, Page 8, Paragraph 0023; Figure 1, Items 1, 2, 3, 5. The multichip memory module includes a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip which are connected during the self-test to store addresses of defective memory cells in the nonvolatile memory chip. *See, e.g.*, Page 8, Paragraph 0023; Figure 1, Items 1, 2, 3, 5. The apparatus also includes a second switching means for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module. *See, e.g.*, Page 7, Paragraph 0022; Figure 1, Items 1, 2, 3, 5. The self-test control means provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip. *See, e.g.*, Page 7, Paragraph 0022; Figure 1, Items 1, 2, 3, 5.

Grounds of Rejection to be Reviewed on Appeal

1. Rejection of claims 1-2, 6 and 11 under 35 U.S.C. 102(e) as being fully anticipated by *Taylor et al.* (U.S. Patent No. 6,971,051, hereinafter, "*Taylor*").

2. Rejection of claims 3-4, 7-8 and 9-10 under 35 U.S.C. 103(a) as being unpatentable over *Taylor*, and further in view of *Barr* (U.S. Patent No. 5,758,056).

3. Rejection of claims 12-15, 17, and 18 under 35 U.S.C. 103(a) as being unpatentable over *Taylor*, and further in view of *Lai et al.* (U.S. Patent No. 5,758,056, hereinafter "*Lai*") and *Barr*.

ARGUMENTS

Rejection of claims 1-2, 6 and 11 under 35 U.S.C. 102(e) anticipated by *Taylor*.

The Applicable Law

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Applicants' Response to Examiner's Rejection

Applicant respectfully submits that *Taylor* fails to disclose that *control signals from outside of the multi-chip memory module are disconnected during a self-test*, as claimed in independent claims 1, 12 and 18. As described in paragraphs [0028]-[0030]. Disconnecting the control signals in this manner allows a common set of terminals of a DRAM, on which the self-test control device is located, to be utilized from the outside, while still preventing access from the outside during the self-test.

Applicant further submits that *Taylor* fails to teach a self-test control device located within a DRAM memory chip, at all. In responding to Applicant's argument, the Examiner cites to the following portion of *Taylor*:

> The self-tester capability includes stored test code that is specific to detecting errors within ***the information (e.g., executable code) residing within the volatile memory***. The stored test code includes instructions which implement memory testing routines. ***The test code may be stored within embedded non-volatile memory of the integrated circuit***. [Emphasis Added] *See Taylor,* Col. 3, Lines 4-9.

The Examiner concludes that "Here, clearly *Taylor et al.* teaches that the self-test capabilities are located within the volatile memory."

Applicant submits, however, that the Examiner has misconstrued the teachings of *Taylor* and that the above-referenced portion states that the self-tester capability is not located within volatile memory, but rather includes executable code *stored in non-volatile memory* used to detect errors *within information residing within the volatile memory*. *See Taylor,* Col. 3, Lines 4-9. In other words, it is the information to be tested that is located in the volatile memory, not the self-tester capability. *See id.* The test code (i.e., the code that performs the test of the information to be tested), on the other hand, is embedded in non-volatile memory. *See id.*

This proper construction is further supported in FIG. 3, which clearly shows TEST CODE ROM 68 that is separate from DRAM 56. *See Taylor,* Figure 3, Items 68, 56. Further, the corresponding description (*see Taylor,* Col. 5, Lines 53-58) clarifies that operation of the self-test capability involves interaction of a processor that executes the self test code contained in TEST CODE ROM 68:

> However, the ASIC does include non-volatile read only memory (ROM) 68 that stores the test code which is used by the processor 58 in performing the self-testing. As a consequence of having the stored test code, printer firmware is able to perform volatile memory checking periodically when the system is inactive. *Taylor,* Col. 5, Lines 53-58.

Thus, the self-test capability taught by *Taylor* clearly is not contained in a DRAM and, further, involves processor interaction. *See id.* This is in stark contrast to the self-test capability claimed in the present application that is located within a DRAM device and relieves a processor from most of the overhead conventionally associated with self-test operations (as described in paragraph [0045]). *See, e.g.,* Claim 1.

For these reasons, Applicant submits that independent Claim 1 as well as their dependents are allowable and respectfully request withdrawal of this rejection.

Rejection of claims 3-4, 7-8 and 9-10 under 35 U.S.C. 103(a) over *Taylor* and further in view of *Barr*.

The Applicable Law

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the first and third criterion.

Applicants' Response to the Examiner's Rejection

Regarding claims 3-4 and 7-10, Applicant submits that these claims depend from Claim 1, which is allowable for reasons discussed above. Accordingly, Applicant submits these claims are also allowable.

Rejection of claims 12-15, 17, and 18 under 35 U.S.C. 103(a) over *Taylor* and further in view of *Lai* and *Barr*.

Regarding claim 12, Applicant submits that the claimed combination of references fail to teach *a self-test control device, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus and a switching device for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module; and wherein the self-test control device provides signals to control inputs of the DRAM memory chip*

and control inputs of the nonvolatile memory chip, as recited in the claim. In other words, even in combination, *Barr* and *Lai* fail to overcome the deficiencies of the teachings of *Taylor*. Thus, Applicant submits claim 12 and its dependents are allowable.

Regarding Claim 18, the Examiner bases the rejection of Claim 18 on the rejection of Claims 1-11 and 12-17 above. Applicants believe the rejection of Claims 1-11 and 12-17 has been overcome as described above. Accordingly, the rejection of Claim 18 is also believed to be overcome, and allowance of the claim is respectfully requested.

CONCLUSION

The Examiner errs in finding that:

1. Claims 1-2, 6 and 11 are anticipated by *Taylor*;

2. Claims 3-4, 7-8 and 9-10 are unpatentable over *Taylor*, and further in view of *Barr*; and

3. Claims 12-15, 17 and 18 are unpatentable over *Taylor,* and further in view of *Lai* and *Bar*.

Withdrawal of the rejections and allowance of all claims is respectfully requested.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

/Randol W. Read, Reg. No. 43,876/

Randol W. Read
Registration No. 43,876
Patterson & Sheridan, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Appellant

CLAIMS APPENDIX

1. (Previously Presented) A method for testing memory cells of a DRAM memory chip arranged together with a non-volatile memory chip in a multichip memory module incorporated in an application apparatus, comprising:

conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus;

providing signals, utilizing a self-test control device located within the DRAM memory chip to a control input of the DRAM memory chip and a control input at the nonvolatile memory chip; and

disconnecting control input signals from outside the multichip memory module using the self-test control device.

2. (Original) The method of claim 1, further comprising:

initiating the self-test by a central processing unit of the application apparatus, the central processing unit arranged outside the multichip memory module.

3. (Original) The method of claim 1, wherein a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip are connected, further comprising:

storing addresses of defective memory cells in the nonvolatile memory chip.

4. (Original) The method of claim 3, further comprising:

deactivating, utilizing a switching device, a common data bus of the DRAM memory chip and the nonvolatile memory chip disposed outside the multichip memory module.

5. (Canceled)

6. (Original) The method of claim 1, further comprising:

selecting addresses of the DRAM memory chip to test memory cells utilizing a self-test control device disposed in the DRAM memory chip.

7. (Original) The method of claim 3, further comprising:

selecting addresses of the nonvolatile memory chip to store the addresses of the defective memory cells of the DRAM memory chip utilizing a central processing unit.

8. (Previously Presented) The method of claims 7, wherein the addresses of the defective memory cells are read from the nonvolatile memory chip by the central processing unit in the operating mode of the application apparatus.

9. (Previously Presented) The method of claim 8, wherein the addresses of the defective memory cells are skipped by an address decoding circuit of the DRAM memory chip during the operating mode of the application apparatus.

10. (Original) The method of claim 1, further comprising:

replacing defective memory cells identified by the self-test with redundant memory cells in the DRAM memory chip.

11. (Original) The method of claim 1, wherein the self-test is conducted in a period from at least one of:

during a battery charging period of the application apparatus;

during a standby period of the application apparatus;

after a battery change of the application apparatus;

after an initial switch-on of the application apparatus;

after a switch-off of the application apparatus; and

according to a time schedule stored in the nonvolatile memory chip.

12. (Previously Presented) An apparatus for testing memory cells of a DRAM memory chip disposed with a nonvolatile memory chip in a multichip memory module incorporated in an application apparatus, comprising:

a self-test control device, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus; and

a second switching device for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory

module; and wherein the self-test control device provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip.

13. (Original) The apparatus of claim 12, further comprising:

a central processing unit, disposed outside the multichip memory module and connected to the self-test control device, for initiating the self-test and providing control commands to the DRAM memory chip.

14. (Original) The apparatus of claim 13, wherein the multichip memory module includes a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip which are connected during the self-test to store addresses of defective memory cells in the nonvolatile memory chip.

15. (Original) The apparatus of claim 14, further comprising:

a switching device for deactivating a common data bus of the DRAM memory chip and of the nonvolatile memory chip outside the multichip memory module.

16. (Canceled)

17. (Original) The apparatus of claim 12, wherein the DRAM memory chip includes redundant memory cells for replacing defective memory cells determined by the self-test.

18. (Previously Presented) An apparatus for testing memory cells of a DRAM memory chip disposed with a nonvolatile memory chip in a multichip memory module incorporated in an application apparatus, comprising:

a self-test control means, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an operating mode of the application apparatus;

a central processing means, disposed outside the multichip memory module and connected to the self-test control device, for initiating the self-test and providing control commands to the DRAM memory chip;

a switching means for deactivating a common data bus of the DRAM memory chip and of the nonvolatile memory chip outside the multichip memory module; and wherein the multichip memory module includes a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip which are connected during the self-test to store addresses of defective memory cells in the nonvolatile memory chip; and

a second switching means for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module; and wherein the self-test control means provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip.

19-21. (Canceled)

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.